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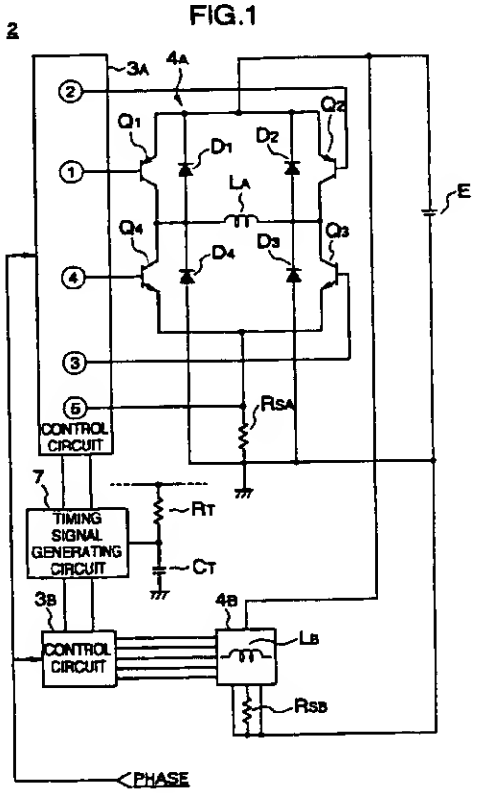
(54) Synchronous driving method for inductive load and synchronous controller for h-bridge circuit

(57) In flowing a switching current through an inductive load (L_A, L_B) by means of an H-bridge circuit (4_A, 4_B), a control circuit (3_A, 3_B) and a timing signal generating circuit (7) are used to start a current supply operation in accordance with a driving period of a predetermined frequency, thereby increasing the current flowing through the inductive load (L_A, L_B). In reducing the current, a power source regeneration operation is performed during a power source regeneration period and a commutation operation is performed during a commutation period. The power source regeneration operation and the commutation operation are well balanced with each other, thereby making it possible to perform a high-frequency driving with a switching current having less ripple. Also, since the power source regeneration operation is performed in a long time in the case where the switching current level is reduced, it becomes possible to quickly reduce the current level down to a desired level.

FIG.1



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the quick attenuation of a current flowing through the inductive load 131 at the time of switching of the current flowing through the inductive load 131 whereas the commutation current 143 can make the slow attenuation thereof.

However, in the case where the release of an energy stored in the inductive load 131 is tried in accordance with any one of the two method mentioned above, a way based on the regeneration current 142 has a demerit that the attenuation is too rapid with the result that the ripple of the switching current flowing through the inductive load 131 is too large. On the other hand, a way based on the commutation current 143 has a demerit that the attenuation is too gentle with the result that the followability in changing a switching current level flowing through the inductive load 131 is poor.

Also, when the driving by a switching current is tried in the case where there are a plurality of above-mentioned inductive loads 131 as in a two-phase stepping motor, there is a problem that in the case where frequencies for controlling respective currents flowing through the plurality of inductive loads are close to each other, beats are generated with the result that poises or vibrations become large.

SUMMARY OF THE INVENTION

The present invention is made in order to solve the above-mentioned inconveniences of the prior art and aims at the provision of a technique with which a switching current flowing through an inductive load can be controlled to the optimum by combining a regeneration current and a commutation current.

Another object of the present invention is to provide a technique with which switching currents flowing through a plurality of inductive loads can be controlled to the optimum.

To solve the above problems, according to one aspect of the present invention, there is provided an inductive load driving method for controlling a current flowing an inductive load, said current being supplied in both forward and reverse directions by an H-bridge circuit including four semiconductor switching elements and flywheel diodes respectively connected to said semiconductor switching elements, said inductive load driving method comprising at least two of a current supplying step of turning two of said semiconductor switching elements on so as to supply a current from a power source to said inductive load; a commutation step of turning one of said semiconductor switching elements on so that energy stored in said inductive load causes a current flowing through said one of said semiconductor switching elements and one of said flywheel diodes; and a power source regeneration step of turning all of said semiconductor switching elements off so that energy stored in said inductive load causes a current flowing through two of said flywheel diodes; wherein said inductive load driving method further comprises the step of generating a timing signal having a predetermined frequency and indicative of a driving period to (i) start said current supplying step in accordance with a start of said driving period and stop said current supplying step when an amplitude of the current flowing though said inductive load becomes a predetermined value or more, (ii) start said power source regeneration step when said current supplying step is stopped before a predetermined time point and stop said power source regeneration step at said predetermined time period, and (iii) start said commutation step when said current supplying step or said current supplying step is stopped and stop said commutation step at an end of said driving period.

Further, according to one aspect of the present invention, there is provided an inductive load driving apparatus comprising: an H-bridge circuit, including four semiconductor switching elements and flywheel diodes respectively connected to said semiconductor switching elements, for supplying a current in both forward and reverse directions through said inductive load; a control circuit for controlling said H-bridge circuit to perform at least two of (i) a current supplying operation of turning two of said semiconductor switching elements on so as to supply a current from a power source to said inductive load, (ii) a power source regeneration operation of turning one of said semiconductor switching elements on so that energy stored in said inductive load causes a current flowing through said one of said semiconductor switching elements and one of said flywheel diodes, and (iii) a commutation operation of turning all of said semiconductor switching elements off so that energy stored in said inductive load causes a current flowing through two of said flywheel diodes; and a timing signal generating circuit for generating a timing signal having a predetermined frequency and indicative of a driving period so that said control circuit controls said H-bridge circuit to (i) start said current supplying operation in accordance with a start of said driving period and stop said current supplying operation when an amplitude of the current flowing though said inductive load becomes a predetermined value or more, (ii) start said power source regeneration operation when said current supplying operation is stopped before a predetermined time point and stop said power source regeneration operation at said predetermined time period, and (iii) start said commutation operation when said current supplying operation or said current supplying operation is stopped and stop said commutation operation at an end of said driving period.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram showing the whole of an inductive load driving apparatus according to the present invention;

Fig. 2 shows the internal block of a control circuit and a timing signal generating circuit of the inductive load driving

The above-mentioned PHASE signal inputted from the exterior is connected to the input terminals of the $NAND_1$ and AND_3, as it is. On the other hand, the PHASE signal is connected to the input terminals of the $NAND_2$ and AND_4 through inverters INV_6 and INV_7, respectively. Thereby, when the PHASE signal is high, the set of the transistors Q_2 and Q_4 are placed into a condition in which they cannot be turned on whereas when the PHASE signal is low, the set of the transistors Q_1 and Q_3 are placed into a condition in which they cannot be turned on. Accordingly, there are neither the simultaneous turn-on of the transistor Q_1 and the transistor Q_4 nor the simultaneous turn-on of the transistor Q_2 and the transistor Q_3. Namely, a control is made so that a through current flowing between the power source E and the ground potential without passing through the inductive load L_A is not generated.

It is now assumed that the PHASE signal takes a high condition so that the turn-on of the transistors Q_2 and Q_4 is inhibited. In this state, the output conditions of the $NAND_1$ and AND_3 change in accordance with signals other than the PHASE signal, thereby controlling the transistors Q_1 and Q_3.

The control circuit 3_A has a reference power source $VREF_1$ for current comparison. The output of the reference $VREF_1$ and the output (⑤) of the current detecting resistor R_{SA} are inputted to an inverted input terminal and a non-inverted input terminal of a comparator $COMP_1$, respectively, and an output terminal of the $COMP_1$ is connected to the set terminal S of each of flip-flops FF_1 and FF_2.

An output terminal Q of the FF_1 is connected to the input terminals of the $NAND_1$ and $NAND_2$ through an INV_2, and an output terminal Q of the FF_2 is connected to the input terminals of the AND_3 and$_4$ through an INV_3.

The truth table of the FF_1 and FF_2 is shown in the following Table 1.

S	R	Q
High	High	Low
High	Low	High
Low	High	Low
Low	Low	Low

Table 1. TRUTH TABLE OF FF_1 AND FF_2

The FF_1 and FF_2 are constructed such that in a state in which the reset terminal R assumes a high condition, the output terminal Q takes a low condition irrespective of the condition of the set terminal S.

Now provided that the output voltage of the current detecting resistor R_{SA} is below the output voltage of the reference power source $VREF_1$, the output of the above-mentioned $COMP_1$ is low and hence the set terminals S of the FF_1 and FF_2 takes low conditions. Accordingly, the output terminals Q of the FF_1 and FF_2 are low. These low outputs are respectively inverted by the INV_2 and INV_3 so that the inverted high outputs are inputted to the $NAND_1$ and $NAND_2$ and the AND_3 and AND_4, respectively.

At this time, since the PHASE signal assumes a high condition, the output of the $NAND_1$ is low and the output of the AND_3 is high. Therefore, the transistors Q_1 and Q_3 are both brought into turned-on conditions.

Thus, in the case where the voltage generated across the current detecting resistor R_{SA} is lower than the output voltage of the $VREF_1$ so that the output of the $COMP_1$ is low and hence the output terminals Q of the FF_1 and FF_2 take low conditions, the transistors Q_1 and Q_3 are turned on so that a current is supplied from the power source E to the inductive load L_A.

When the voltage supplied from the power source E increases so that the voltage generated across the current detecting resistor R_{SA} exceeds the output voltage of the $VREF_1$, the output of the $COMP_1$ is inverted from the low condition to a high condition. Thereby, the set terminals S of the FF_1 and FF_2 turn into high conditions.

As shown in Table 1 mentioned above, the FF_1 and FF_2 are constructed such that the condition of the output terminal Q can be controlled in accordance with the condition of the reset terminal R even if the set terminal S takes a high condition. The reset terminals R of the FF_1 and FF_2 are connected to the output terminals of the timing signal generating circuit 7. As a result, the output terminals Q of the FF_1 and FF_2 are controlled by the timing signal generating circuit 7 when the output of the $COMP_1$ is high.

Explaining the internal block of the timing signal generating circuit 7, the timing signal generating circuit 7 has an oscillator OSC, a comparator $COMP_2$, a reference power source $VREF_2$ and an OR_1 and a connection is made such that the voltage of the above-mentioned timing condenser C_T is inputted to the OSC.

The OSC has a circuit incorporated therein for charging and discharging the timing condenser C_T. With the opera-

are both turned on so that there is performed a current supply operation in which a current is supplied from the power source E to the inductive load L_A.

If the reset terminal R takes the high condition, the output terminal Q takes the low condition irrespective of the condition of the set terminal S. Therefore, during the time when the rectangular wave 22 is high, the output terminals Q of the FF_1 and FF_2 take the low conditions irrespective of whether the condition of the output signal of the $COMP_1$ is high or low, that is, in either the case where a voltage generated across the current detecting resistor R_{SA} exceeds the output voltage of the $VREF_1$ or the case where the former voltage is below the latter voltage. As a result, the turned-on conditions of the transistors Q_1 and Q_3 are kept.

Provided that a period of time when the rectangular wave 22 is high is called a "compulsory turn-on period", the forced turn-on period corresponds to a period of time when the voltage of the sawtooth wave 21 attenuates. Also, the forced turn-on period corresponds to an initial stage of start of the current supply operation. When the current supply operation is started, there is the case where noises are generated by a through current which may flow in a reverse recovery time of the flywheel diode D_1 or D_2 or a through current which may flow due to a capacitance component of the inductive load L_A. However, the initial period of start of the current supply operation is taken as the forced turn-on period, thereby ignoring the output of the $COMP_1$. Therefore, even in the case where the output of the $COMP_1$ is inverted by the noises, there is no fear that an erroneous operation of erroneously stopping the current supply operation is generated.

When the forced turn-on period is completed, the rectangular wave 22 and the rectangular wave 24 turn into low conditions and hence the reset terminals R of the FF_1 and FF_2 are brought into low conditions. The condition of the output terminal Q of the FF_1 or FF_2 is determined in accordance with the condition of the set terminal S when the condition of the reset terminal R is low. Accordingly, in the case where the output of the $COMP_1$ has taken a high condition as the result of the increase of a current supplied from the power source E in the compulsory turn-on period, the output terminals Q of the FF_1 and FF_2 immediately turn into high conditions, thereby bringing the transistors Q_1 and Q_3 into turned-off conditions.

On the other hand, in the case where the output of the $COMP_1$ is low at a point of time when the compulsory turn-on period is completed, the conditions of the output terminals Q of the FF_1 and FF_2 remain as they were low and the transistors Q_1 and Q_3 maintain the turned-on conditions. In time, however, the current supplied from the power source E to the inductive load L_A increases so that the output of the $COMP_1$ is inverted.

In this case, since the condition of the rectangular wave 22 is low and hence the condition of the reset terminal R of the FF_1 is low, the output terminal Q of the FF_1 turns into a high condition in accordance with the inversion of the output of the $COMP_1$, thereby turning the transistor Q_1 off. But, a state of the reset terminal R of the FF_2 differs in accordance with the condition of the rectangular wave 24.

Assume that a period of time from the start of a compulsory turn-on period until the turn of the rectangular wave 24 from a low condition into a high condition is called a power source regeneration period and a period of time from the turn of the rectangular wave 24 into the high condition until the start of a forced turn-on period in the next driving period T is called a commutation period. In the case where the output of the $COMP_1$ is inverted in the power source regeneration period, the output terminal Q of the FF_2 turns from a low condition into a high condition and hence the transistor Q_3 is also turned off so that a power source regeneration operation is started. When a commutation period is started after the power regeneration period is completed, the transistor Q_3 is turned on again so that the power source regeneration operation transfers to a commutation operation.

Then, a current is supplied from the power source E to the inductive load L_A by virtue of a current supply operation. Thus, the power source regeneration operation and the commutation operation are performed in a well-balanced manner.

In this way, the operation differs in accordance with whether the point of time of inversion of the output of the $COMP_1$ is in the power source regeneration period or in the commutation period. Therefore, more detailed explanation will be made by use of Fig. 3 with the A and B phases of the two-phase stepping motor being applied to the former and latter cases, respectively. Herein, it is assumed that currents flowing through the A-phase and B-phase inductive loads L_A and L_B are I_{LA} and I_{LB} respectively and the values of the output voltages of the $VREF_1$'s in the control circuits 3_A and 3_B reduced to current values are $IREF_A$ and $IREF_B$ respectively.

First, it is assumed that the currents flowing through the inductive loads L_A and L_B begin to increase at a point (P11 or P21) of time of turn of the rectangular wave 22 from a low condition into a high condition, and the current I_{LA} flowing through the A-phase inductive load L_A reaches the upper limit current $IREF_A$ (or a current having an amplitude with which the $COMP_2$ is inverted) at a point P_{12} in a power source regeneration period when the condition of the rectangular wave 24 is low whereas the current I_{LB} flowing through the B-phase inductive load L_B reaches the upper limit current $IREF_B$ at a point P_{22} in a commutation period when the condition of the rectangular wave 24 is high.

In such circumstances, the output of the $COMP_1$ in the control circuit 3A is first inverted from a low condition to a high condition at the point of time P12 when the current I_{LA} flowing through the inductive load L_A reaches $IREF_A$. Thereby, the set terminals S of the FF_1 and FF_2 in the control circuit 3_A turn into a high condition. In the power source

As explained in the foregoing, the start of a current supply operation for the A-phase inductive load L_A and the start of a current supply operation for the B-phase inductive load L_B are determined by the time constant of one series circuit of the timing resistor R_T and the timing condenser C_T and one timing signal generating circuit 7 and are therefore simultaneous with each other. Accordingly, there is no fear that the timings of start of both the current supply operations deviate from each other. As a result, there is no fear that noises or vibrations caused by beats are generated.

The above-mentioned series of operations concern the case where currents flown to the inductive loads L_A and L_B are switched to keep the values thereof constant. In the inductive load driving apparatus 2, however, the amplitudes of switching currents flown to the inductive loads L_A and L_B can be changed by changing the output voltages of the reference power sources $VREF_1$ and $VREF_2$ for current comparison in the control circuits 3_A and 3_B.

The change of the flown switching current will be explained in Fig. 4 with the A-phase inductive load L_A taken as an example. Herein, it is assumed that from a steady state in which a constant level of the current $IREF_A$ is maintained, the switching current flowing through the inductive load L_A is changed to $IREF'_A$ at a point P31 of time by reducing the output voltage of the reference power source $VREF_1$ for current comparison.

Each of the current levels $IREF_A$ and $IREF'_A$ is a current value with which the output of the $COMP_1$ in the control circuit 3_A is inverted. Assume that at a point of time of completion of a compulsory turn-on period, a current flowing through the inductive load L_A has already exceeded $IREF'_A$ and the $COMP_1$ has taken a high condition. At the point of time of completion of the forced turn-on period, the transfer to a power source regeneration operation is immediately made. When there turns into a commutation period, the transfer from the power source regeneration operation to a commutation operation is made.

In the case where there transfers from that state to a current supply operation, it is general that the current I_{LA} flowing through the inductive load L_A remains over $IREF'_A$ and hence the transfer to the power source regeneration operation is made immediately after the completion of a compulsory turn-on period.

The above operation is repeated until the current I_{LA} flowing through the inductive load L_A at the point of time of completion of a compulsory turn-on period is below $IREF'_A$.

Even in such a transient state, a current is supplied from the power source E. This is made for causing the flow of a current through the current detecting resistor R_{SA} to detect the amplitude of the current I_{LA} through the inductive load L_A so that the return to a steady state is immediately made when the current I_{LA} is below the current $IREF'_A$ which is a reference current.

Also in this transient state, the driving period T follows the oscillating period of the sawtooth wave 21 as in the steady state with no difference between the transient state and the steady state. The operations for the A and B phases are synchronous with each other so that a current supply operation, a power source regeneration operation and a commutation operation for the A phase are started simultaneously with those for the B phase, respectively.

On the other hand, in the transient operation, the transfer to the power source regeneration operation is made immediately after the completion of the compulsory turn-on period, unlike the steady state. Therefore, a period of time in one driving period T when the power source regeneration operation is performed is long as compared with that in the steady state. Accordingly, the current I_{LA} flowing through the inductive load L_A rapidly attenuates, thereby enabling the quick arrival to the intended current $IREF'_A$.

In the above-mentioned inductive load driving apparatus 2, bi-polar transistors are used as the semiconductor switching elements. However, insulated gate transistors (MOSFET's) may be used. The flywheel diodes may include various rectifying elements such as pn junction diodes, Schottky diodes or the like.

Though the above-mentioned inductive load driving apparatus 2 has an IC structure, the present invention may include a multi-chip module having the transistors Q_1 to Q_4 and the flywheel diodes D_1 to D_4 as single chips and a hybrid IC.

Inversely, a structure having the timing resistor R_T and the current detecting resistor R_S incorporated therein may also be included in the present invention.

Since a power source regeneration operation and a commutation operation can be performed in a well-balanced manner, a high-frequency driving can be performed with a switching current having a small ripple.

Even if a plurality of inductive loads are driven, there is no fear that noises or vibrations caused by beats are generated.

When a switching current level flown to an inductive load is to be reduced, the reduction can be made quickly.

Claims

1. An inductive load driving method for controlling a current flowing an inductive load (L_A), said current being supplied in both forward and reverse directions by an H-bridge circuit (4_A) including four semiconductor switching elements (Q_1-Q_4) and flywheel diodes (D_1-D_4) respectively connected to said semiconductor switching elements, said inductive load driving method comprising at least two of:

FIG.1

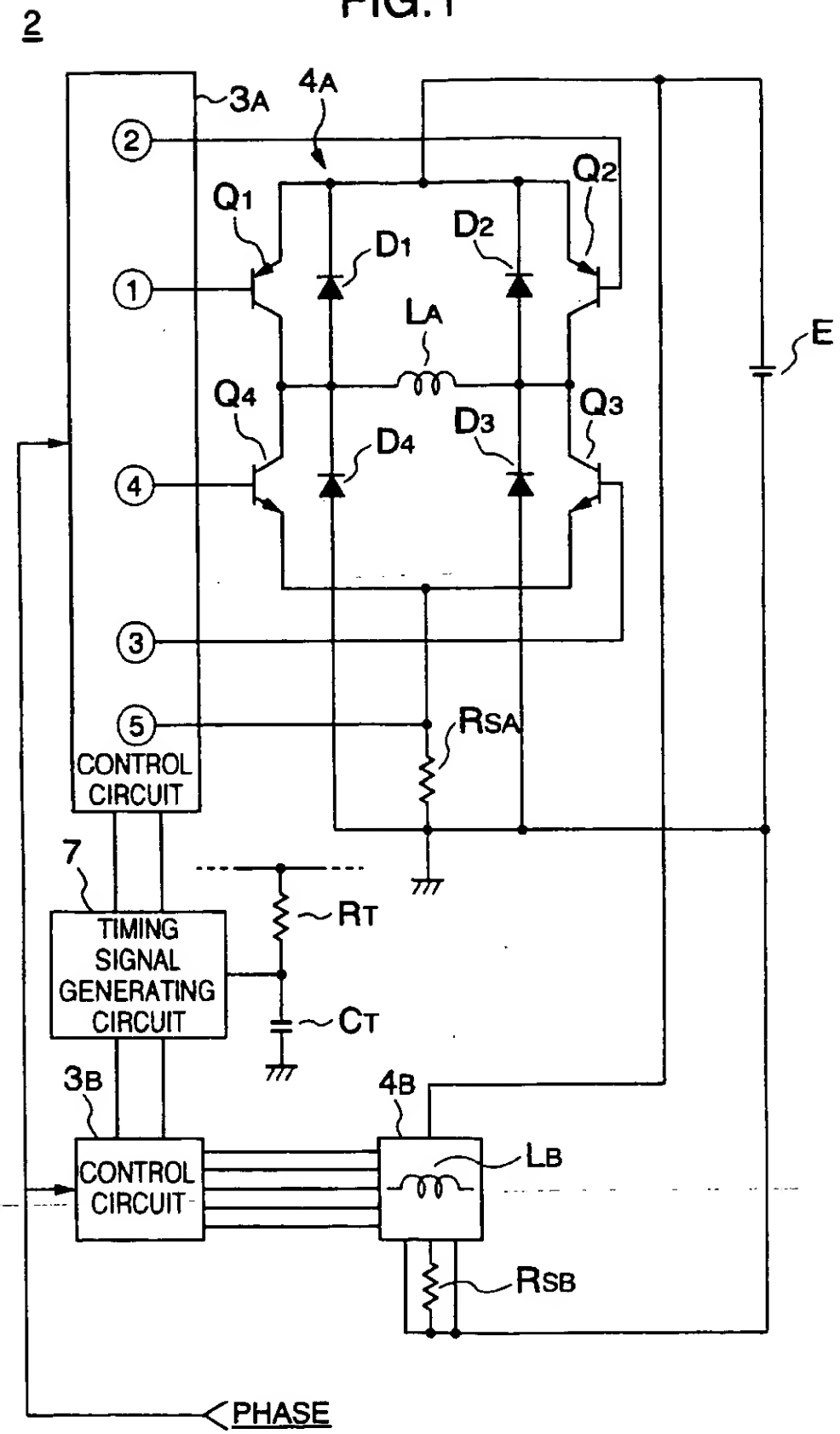
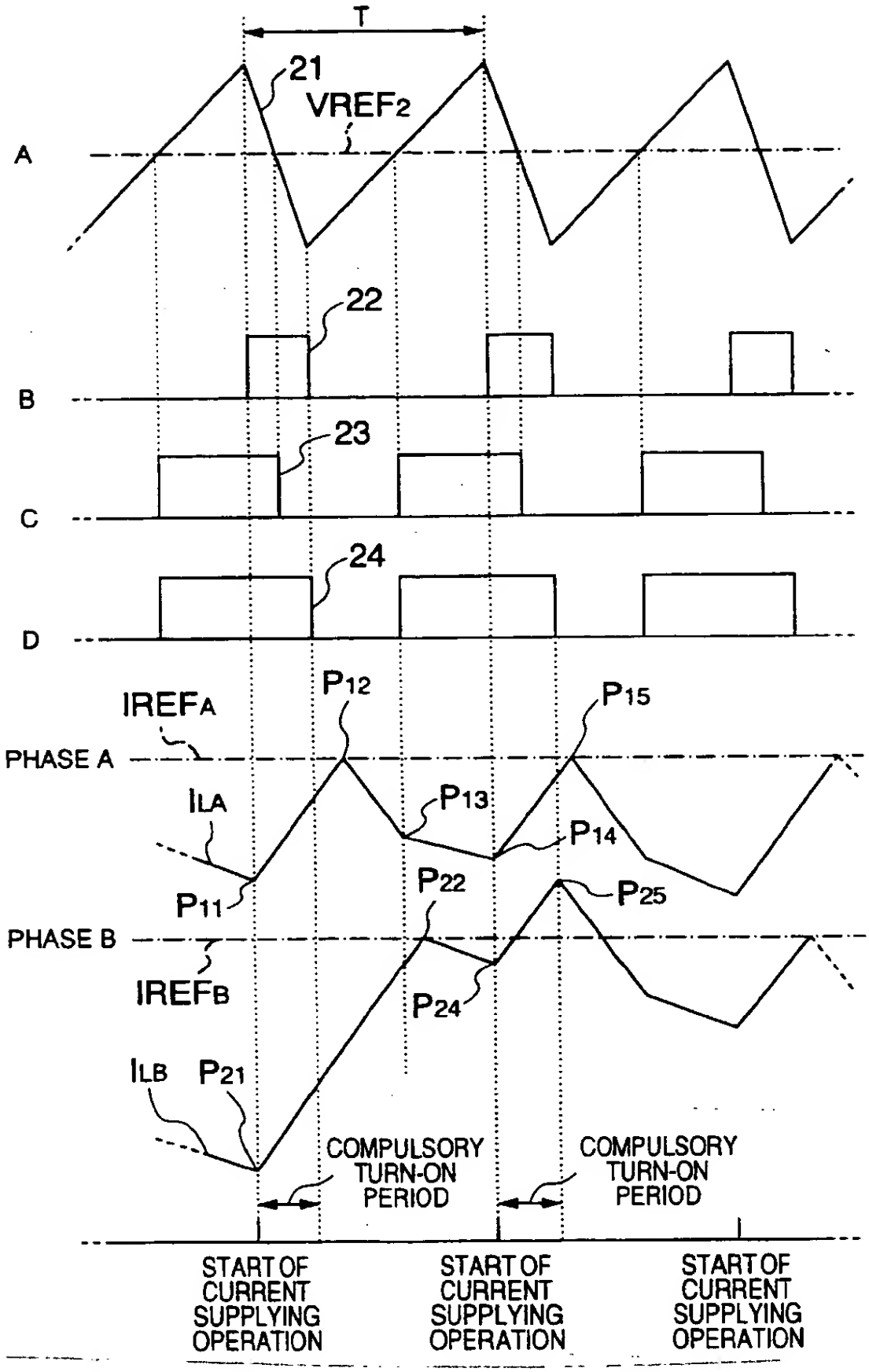

2
3A
4A
Q1
Q2
D1
D2
LA
E
Q4
Q3
D4
D3
RSA
CONTROL CIRCUIT
7
TIMING SIGNAL GENERATING CIRCUIT
RT
CT
3B
4B
CONTROL CIRCUIT
LB
RSB
PHASE

FIG.3


T
21
VREF2
A
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B
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C
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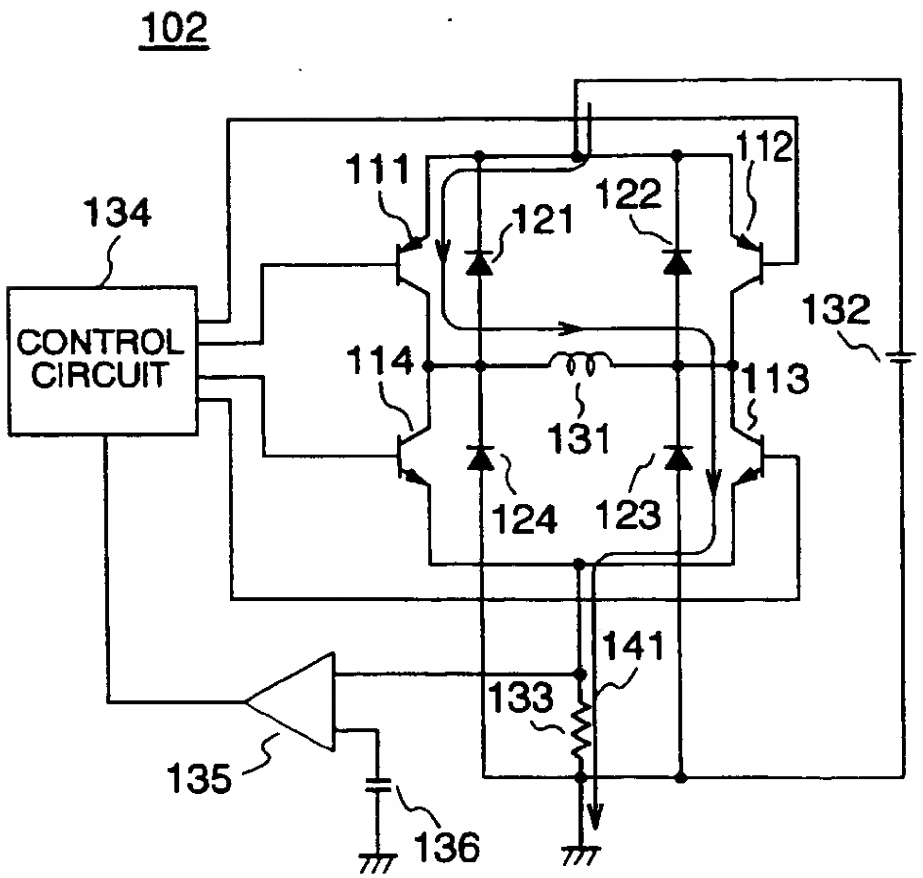
D
IREFA
P12
P15
PHASE A
ILA
P13
P14
P11
P22
P25
PHASE B
IREFB
P24
ILB
P21
COMPULSORY TURN-ON PERIOD
COMPULSORY TURN-ON PERIOD
START OF CURRENT SUPPLYING OPERATION
START OF CURRENT SUPPLYING OPERATION
START OF CURRENT SUPPLYING OPERATION

FIG.5


102
134
CONTROL CIRCUIT
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EUROPEAN SEARCH REPORT

Application Number EP 97113903.5

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl. 6)
A	US 5032780 A (HOPKINS) 16 July 1991 (16.07.91), column 1, line 37 - column 3, line 61, column 4, line 15 - column 5, line 32, fig. 1-3. --	1,2,4, 5	H 02 P 8/12
A	Patent Abstracts of Japan, Vol. 95, No. 5, 30 June 1995; & JP 7-39194 A (FUJITSU), 07 February 1995. --	1,2,4, 5	
A	EP 0196543 A2 (KOLLMORGEN TECHNOLOGIES) 08 October 1986 (08.10.86), abstract, page 4, line 27 - page 7, line 8, fig. 1-5. ----	1,4	

TECHNICAL FIELDS SEARCHED (Int. Cl. 6)

H 02 P

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
VIENNA	18-12-1997	HAJOS

CATEGORY OF CITED DOCUMENTS

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